

Please type a plus sign (+) inside this box →

PTO/SB/05 (12/97)
Approved for use through 09/30/00. OMB 0651-0032
Remark Office: U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

<p align="center">UTILITY PATENT APPLICATION TRANSMITTAL</p> <p align="center"><i>(Only for new nonprovisional applications under 37 CFR 1.53(b))</i></p>	Attorney Docket No.	042390.P5769	Total Pages	22
	First Named Inventor or Application Identifier			
	Gang Bai			
	Express Mail Label No.	EM014063345US		

APPLICATION ELEMENTS <i>See MPEP chapter 600 concerning utility patent application contents</i>		ADDRESS TO: Assistant Commissioner for Patents Box Patent Application Washington, DC 20231	
<div style="margin-bottom: 10px;"> 1. <input checked="" type="checkbox"/> Fee Transmittal Form <i>(Submit an original, and a duplicate for fee processing)</i> </div> <div style="margin-bottom: 10px;"> 2. <input checked="" type="checkbox"/> Specification [Total Pages 18] <i>(preferred arrangement set forth below)</i> <ul style="list-style-type: none"> - Descriptive title of the Invention - Cross References to Related Applications - Statement Regarding Fed sponsored R & D - Reference to Microfiche Appendix - Background of the Invention - Brief Summary of the Invention - Brief Description of the Drawings <i>(if filed)</i> - Detailed Description - Claim(s) - Abstract of the Disclosure </div> <div style="margin-bottom: 10px;"> 3. <input checked="" type="checkbox"/> Drawing(s) (35 CFR 113) [Total Sheets 1] </div> <div style="margin-bottom: 10px;"> 4. Oath or Declaration [Total Pages] <ul style="list-style-type: none"> a. <input type="checkbox"/> Newly executed (original copy) b. <input type="checkbox"/> Copy from a prior application (37 CFR 1.63(d)) <i>(for continuation disclosure with Box 17 completed)</i> [Note Box 5 below] i. <input type="checkbox"/> DELETION OF INVENTOR(S) Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b). </div> <div> 5. <input type="checkbox"/> Incorporation By Reference (usable if Box 4b is checked) The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein. </div>	<div style="margin-bottom: 10px;"> 6. <input type="checkbox"/> Microfiche Computer Program (Appendix) </div> <div> 7. Nucleotide and/or Amino Acid Sequence Submission <i>(if applicable, all necessary)</i> <ul style="list-style-type: none"> a. <input type="checkbox"/> Computer Readable Copy b. <input type="checkbox"/> Paper Copy (identical to computer copy) c. <input type="checkbox"/> Statement verifying identity of above copies </div>		
ACCOMPANYING APPLICATION PARTS			
<div style="margin-bottom: 10px;"> 8. <input type="checkbox"/> Assignment Papers (cover sheet & document(s)) </div> <div style="margin-bottom: 10px;"> 9. <input type="checkbox"/> 37 CFR 3.73(b) Statement <input type="checkbox"/> Power of Attorney <i>(when there is an assignee)</i> </div> <div style="margin-bottom: 10px;"> 10. <input type="checkbox"/> English Translation Document (if applicable) </div> <div style="margin-bottom: 10px;"> 11. <input type="checkbox"/> Information Disclosure Statement (IDS)/PTO - 1449 <input type="checkbox"/> Copies of IDS Citations </div> <div style="margin-bottom: 10px;"> 12. <input type="checkbox"/> Preliminary Amendment </div> <div style="margin-bottom: 10px;"> 13. <input checked="" type="checkbox"/> Return Receipt Postcard (MPEP 503) <i>(Should be specifically itemized)</i> </div> <div style="margin-bottom: 10px;"> 14. <input type="checkbox"/> Small Entity Statement(s) <input type="checkbox"/> Statement filed in prior application, Status still proper and desired </div> <div style="margin-bottom: 10px;"> 15. <input type="checkbox"/> Certified Copy of Priority Document(s) <i>(if foreign priority is claimed)</i> </div> <div> 16. <input type="checkbox"/> Other: </div>			
17. If a CONTINUING APPLICATION, check appropriate box and supply the requisite information: <input type="checkbox"/> Continuation <input type="checkbox"/> Divisional <input type="checkbox"/> Continuation-in-part (CIP) of prior application No: _____ / _____			
18. CORRESPONDENCE ADDRESS			
<div style="display: flex; align-items: center;"> <input type="checkbox"/> Customer Number of Bar Code Label <div style="border: 1px dashed black; flex-grow: 1; text-align: center; padding: 10px; margin: 0 10px;"> <i>(Insert Customer No. or Attach bare code label here)</i> </div> or <input checked="" type="checkbox"/> Correspondence address below </div>			
NAME	BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP		
ADDRESS	12400 Wilshire Boulevard, Seventh Floor		
CITY	Los Angeles	STATE	California
COUNTRY	U.S.A.	TELEPHONE	(310) 207-3800
		ZIP CODE	90025
		FAX	(310) 820-5988

Burden Hour Statement. This form is estimated to take 0.2 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Assistant Commissioner for Patents, Box Patent Application, Washington, DC 20231.

06/30/98

1587 U.S. PTO

FEE TRANSMITTAL <i>Note: Effective October 1, 1997. Patent fees are subject to annual revision.</i>		Complete if Known		
		Application Number		
		Filing Date	06/30/98	
		First Named Inventor	Gang Bai	
		Group Art Unit		
TOTAL AMOUNT OF PAYMENT (\$)		790.00	Examiner Name	
			Attorney Docket Number	042390.P5769

METHOD OF PAYMENT (check one)		FEE CALCULATION (continued)																																																																																																																																																																									
1. <input checked="" type="checkbox"/> The Commissioner is hereby authorized to charge indicated fees and credit any over payments to: Deposit Account Number: 02-2666 Deposit Account Name: Blakely, Sokoloff, Taylor & Zafman LLP <input checked="" type="checkbox"/> Charge Any Additional Fee Required Under 37 CFR 1.16 and 1.17 <input type="checkbox"/> Charge the Issue Fee Set in 37 CFR 1.18 at the Mailing of the Notice of Allowance, 37 CFR 1.311(b)		3. ADDITIONAL FEE <table border="1"> <thead> <tr> <th>Large Fee Code</th> <th>Entity Fee (\$)</th> <th>Small Fee Code</th> <th>Entity Fee (\$)</th> <th>Fee Description</th> <th>Fee Paid</th> </tr> </thead> <tbody> <tr><td>105</td><td>130</td><td>205</td><td>65</td><td>Surcharge - late filing fee or oath</td><td></td></tr> <tr><td>127</td><td>50</td><td>227</td><td>25</td><td>Surcharge - late provisional filing fee or cover sheet</td><td></td></tr> <tr><td>139</td><td>130</td><td>139</td><td>130</td><td>Non-English specification</td><td></td></tr> <tr><td>147</td><td>2,520</td><td>147</td><td>2,520</td><td>For filing a request for reexamination</td><td></td></tr> <tr><td>112</td><td>920</td><td>112</td><td>920</td><td>Requesting publication of SIR prior to Examiner action</td><td></td></tr> <tr><td>113</td><td>1,840</td><td>113</td><td>1,840</td><td>Requesting publication of SIR after Examiner action</td><td></td></tr> <tr><td>115</td><td>110</td><td>215</td><td>55</td><td>Extension for response within first month</td><td></td></tr> <tr><td>116</td><td>400</td><td>216</td><td>200</td><td>Extension for response within second month</td><td></td></tr> <tr><td>117</td><td>950</td><td>217</td><td>475</td><td>Extension for response within third month</td><td></td></tr> <tr><td>118</td><td>1,510</td><td>218</td><td>755</td><td>Extension for response within fourth month</td><td></td></tr> <tr><td>119</td><td>310</td><td>219</td><td>155</td><td>Notice of Appeal</td><td></td></tr> <tr><td>120</td><td>310</td><td>220</td><td>155</td><td>Filing a brief in support of an appeal</td><td></td></tr> <tr><td>121</td><td>270</td><td>221</td><td>135</td><td>Request for oral hearing</td><td></td></tr> <tr><td>138</td><td>1,510</td><td>138</td><td>1,510</td><td>Petition to institute a public use proceeding</td><td></td></tr> <tr><td>140</td><td>110</td><td>240</td><td>55</td><td>Petition to revive unavoidably abandoned application</td><td></td></tr> <tr><td>141</td><td>1,320</td><td>241</td><td>660</td><td>Petition to revive unintentionally abandoned application</td><td></td></tr> <tr><td>142</td><td>1,320</td><td>242</td><td>660</td><td>Utility issue fee (or reissue)</td><td></td></tr> <tr><td>143</td><td>450</td><td>243</td><td>225</td><td>Design issue fee</td><td></td></tr> <tr><td>144</td><td>670</td><td>244</td><td>335</td><td>Plant issue fee</td><td></td></tr> <tr><td>122</td><td>130</td><td>122</td><td>130</td><td>Petitions to the Commissioner</td><td></td></tr> <tr><td>123</td><td>50</td><td>123</td><td>50</td><td>Petitions related to provisional applications</td><td></td></tr> <tr><td>126</td><td>240</td><td>126</td><td>240</td><td>Submission of Information Disclosure Stmt</td><td></td></tr> <tr><td>581</td><td>40</td><td>581</td><td>40</td><td>Recording each patent assignment per property (times number of properties)</td><td></td></tr> <tr><td>146</td><td>790</td><td>246</td><td>395</td><td>Filing a submission after final rejection (37 CFR 1.129(a))</td><td></td></tr> <tr><td>149</td><td>790</td><td>249</td><td>395</td><td>For each additional invention to be examined (37 CFR 1.129(b))</td><td></td></tr> <tr><td colspan="5">Other fee (specify) _____</td><td></td></tr> <tr><td colspan="5">Other fee (specify) _____</td><td></td></tr> </tbody> </table>		Large Fee Code	Entity Fee (\$)	Small Fee Code	Entity Fee (\$)	Fee Description	Fee Paid	105	130	205	65	Surcharge - late filing fee or oath		127	50	227	25	Surcharge - late provisional filing fee or cover sheet		139	130	139	130	Non-English specification		147	2,520	147	2,520	For filing a request for reexamination		112	920	112	920	Requesting publication of SIR prior to Examiner action		113	1,840	113	1,840	Requesting publication of SIR after Examiner action		115	110	215	55	Extension for response within first month		116	400	216	200	Extension for response within second month		117	950	217	475	Extension for response within third month		118	1,510	218	755	Extension for response within fourth month		119	310	219	155	Notice of Appeal		120	310	220	155	Filing a brief in support of an appeal		121	270	221	135	Request for oral hearing		138	1,510	138	1,510	Petition to institute a public use proceeding		140	110	240	55	Petition to revive unavoidably abandoned application		141	1,320	241	660	Petition to revive unintentionally abandoned application		142	1,320	242	660	Utility issue fee (or reissue)		143	450	243	225	Design issue fee		144	670	244	335	Plant issue fee		122	130	122	130	Petitions to the Commissioner		123	50	123	50	Petitions related to provisional applications		126	240	126	240	Submission of Information Disclosure Stmt		581	40	581	40	Recording each patent assignment per property (times number of properties)		146	790	246	395	Filing a submission after final rejection (37 CFR 1.129(a))		149	790	249	395	For each additional invention to be examined (37 CFR 1.129(b))		Other fee (specify) _____						Other fee (specify) _____					
Large Fee Code	Entity Fee (\$)	Small Fee Code	Entity Fee (\$)	Fee Description	Fee Paid																																																																																																																																																																						
105	130	205	65	Surcharge - late filing fee or oath																																																																																																																																																																							
127	50	227	25	Surcharge - late provisional filing fee or cover sheet																																																																																																																																																																							
139	130	139	130	Non-English specification																																																																																																																																																																							
147	2,520	147	2,520	For filing a request for reexamination																																																																																																																																																																							
112	920	112	920	Requesting publication of SIR prior to Examiner action																																																																																																																																																																							
113	1,840	113	1,840	Requesting publication of SIR after Examiner action																																																																																																																																																																							
115	110	215	55	Extension for response within first month																																																																																																																																																																							
116	400	216	200	Extension for response within second month																																																																																																																																																																							
117	950	217	475	Extension for response within third month																																																																																																																																																																							
118	1,510	218	755	Extension for response within fourth month																																																																																																																																																																							
119	310	219	155	Notice of Appeal																																																																																																																																																																							
120	310	220	155	Filing a brief in support of an appeal																																																																																																																																																																							
121	270	221	135	Request for oral hearing																																																																																																																																																																							
138	1,510	138	1,510	Petition to institute a public use proceeding																																																																																																																																																																							
140	110	240	55	Petition to revive unavoidably abandoned application																																																																																																																																																																							
141	1,320	241	660	Petition to revive unintentionally abandoned application																																																																																																																																																																							
142	1,320	242	660	Utility issue fee (or reissue)																																																																																																																																																																							
143	450	243	225	Design issue fee																																																																																																																																																																							
144	670	244	335	Plant issue fee																																																																																																																																																																							
122	130	122	130	Petitions to the Commissioner																																																																																																																																																																							
123	50	123	50	Petitions related to provisional applications																																																																																																																																																																							
126	240	126	240	Submission of Information Disclosure Stmt																																																																																																																																																																							
581	40	581	40	Recording each patent assignment per property (times number of properties)																																																																																																																																																																							
146	790	246	395	Filing a submission after final rejection (37 CFR 1.129(a))																																																																																																																																																																							
149	790	249	395	For each additional invention to be examined (37 CFR 1.129(b))																																																																																																																																																																							
Other fee (specify) _____																																																																																																																																																																											
Other fee (specify) _____																																																																																																																																																																											
FEE CALCULATION (fees effective 10/01/96)																																																																																																																																																																											
1. FILING FEE <table border="1"> <thead> <tr> <th>Large Fee Code</th> <th>Entity Fee (\$)</th> <th>Small Fee Code</th> <th>Entity Fee (\$)</th> <th>Fee Description</th> <th>Fee Paid</th> </tr> </thead> <tbody> <tr><td>101</td><td>790</td><td>201</td><td>395</td><td>Utility filing fee</td><td>\$790</td></tr> <tr><td>106</td><td>330</td><td>206</td><td>165</td><td>Design filing fee</td><td></td></tr> <tr><td>107</td><td>540</td><td>207</td><td>270</td><td>Plant filing fee</td><td></td></tr> <tr><td>108</td><td>790</td><td>208</td><td>395</td><td>Reissue filing fee</td><td></td></tr> <tr><td>114</td><td>150</td><td>214</td><td>75</td><td>Provisional filing fee</td><td></td></tr> <tr><td colspan="5">SUBTOTAL (1)</td><td>(\$) 790.00</td></tr> </tbody> </table>		Large Fee Code	Entity Fee (\$)	Small Fee Code	Entity Fee (\$)	Fee Description	Fee Paid	101	790	201	395	Utility filing fee	\$790	106	330	206	165	Design filing fee		107	540	207	270	Plant filing fee		108	790	208	395	Reissue filing fee		114	150	214	75	Provisional filing fee		SUBTOTAL (1)					(\$) 790.00																																																																																																																																
Large Fee Code	Entity Fee (\$)	Small Fee Code	Entity Fee (\$)	Fee Description	Fee Paid																																																																																																																																																																						
101	790	201	395	Utility filing fee	\$790																																																																																																																																																																						
106	330	206	165	Design filing fee																																																																																																																																																																							
107	540	207	270	Plant filing fee																																																																																																																																																																							
108	790	208	395	Reissue filing fee																																																																																																																																																																							
114	150	214	75	Provisional filing fee																																																																																																																																																																							
SUBTOTAL (1)					(\$) 790.00																																																																																																																																																																						
2. CLAIMS <table border="1"> <thead> <tr> <th>Total Claims</th> <th>Extra</th> <th>Fee from below</th> <th>Fee Paid</th> </tr> </thead> <tbody> <tr> <td>14</td> <td>-20 = 0</td> <td>X \$22.00 =</td> <td>0.00</td> </tr> <tr> <td>Independent Claims</td> <td>2</td> <td>-3 = 0</td> <td>X \$82.00 =</td> <td>0.00</td> </tr> <tr> <td>Multiple Dependent Claims</td> <td></td> <td></td> <td></td> </tr> </tbody> </table>		Total Claims	Extra	Fee from below	Fee Paid	14	-20 = 0	X \$22.00 =	0.00	Independent Claims	2	-3 = 0	X \$82.00 =	0.00	Multiple Dependent Claims																																																																																																																																																												
Total Claims	Extra	Fee from below	Fee Paid																																																																																																																																																																								
14	-20 = 0	X \$22.00 =	0.00																																																																																																																																																																								
Independent Claims	2	-3 = 0	X \$82.00 =	0.00																																																																																																																																																																							
Multiple Dependent Claims																																																																																																																																																																											
<table border="1"> <thead> <tr> <th>Large Fee Code</th> <th>Entity Fee (\$)</th> <th>Small Fee Code</th> <th>Entity Fee (\$)</th> <th>Fee Description</th> <th>Fee Paid</th> </tr> </thead> <tbody> <tr><td>103</td><td>22</td><td>203</td><td>11</td><td>Claims in excess of 20</td><td></td></tr> <tr><td>102</td><td>82</td><td>202</td><td>41</td><td>Independent claims in excess of 3</td><td></td></tr> <tr><td>104</td><td>270</td><td>204</td><td>135</td><td>Multiple Dependent claim</td><td></td></tr> <tr><td>109</td><td>82</td><td>209</td><td>41</td><td>Reissue independent claims over original patent</td><td></td></tr> <tr><td>110</td><td>22</td><td>210</td><td>11</td><td>Reissue claims in excess of 20 and over original patent</td><td></td></tr> <tr><td colspan="5">SUBTOTAL (2)</td><td>(\$) 0.00</td></tr> </tbody> </table>		Large Fee Code	Entity Fee (\$)	Small Fee Code	Entity Fee (\$)	Fee Description	Fee Paid	103	22	203	11	Claims in excess of 20		102	82	202	41	Independent claims in excess of 3		104	270	204	135	Multiple Dependent claim		109	82	209	41	Reissue independent claims over original patent		110	22	210	11	Reissue claims in excess of 20 and over original patent		SUBTOTAL (2)					(\$) 0.00																																																																																																																																
Large Fee Code	Entity Fee (\$)	Small Fee Code	Entity Fee (\$)	Fee Description	Fee Paid																																																																																																																																																																						
103	22	203	11	Claims in excess of 20																																																																																																																																																																							
102	82	202	41	Independent claims in excess of 3																																																																																																																																																																							
104	270	204	135	Multiple Dependent claim																																																																																																																																																																							
109	82	209	41	Reissue independent claims over original patent																																																																																																																																																																							
110	22	210	11	Reissue claims in excess of 20 and over original patent																																																																																																																																																																							
SUBTOTAL (2)					(\$) 0.00																																																																																																																																																																						

* Reduced by Basic Filing Fee Paid

SUBMITTED BY		Complete (if applicable)	
Typed or Printed Name	William Thomas Babbitt, Reg. No. 39,591	Reg. Number	
Signature	<i>William T Babbitt</i>	Date	6/30/98
		Deposit Account User ID	02-2666

Burden Hour Statement: This form is estimated to take 0.2 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Assistant Commissioner for Patents, Box Patent Application, Washington, DC 20231.

Attorney's Docket No. 042390.P5769
Express Mail No. EM014063345US

UNITED STATES PATENT APPLICATION

FOR

A MULTI-LAYER GATE DIELECTRIC

Inventor:

Gang Bai

Prepared by:

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN, LLP
12400 Wilshire Boulevard, Seventh Floor
Los Angeles, California 90025
(310) 207-3800

BACKGROUND OF THE INVENTION

Field of the Invention

The invention relates to integrated circuit devices and more particularly to enhancing dielectric material in those device.

Description of Related Art

One way to improve integrated circuit performance is through scaling the individual devices that comprise the integrated circuit. Thus, each subsequent generation of integrated circuit generally involves reducing the size of the individual devices on, for example, a semiconductor chip. The Morse rule is a common benchmark in the integrated circuit technology and provides that devices will be scaled down or reduced in size by one-third for each new generation.

The scale of a transistor device requires consideration of the desired performance of the device. For example, one goal may be to increase the current flow in the semiconductor material of the transistor. The current flow is proportional to the voltage applied to the gate electrode and the capacitance seen at the gate:

$$Q \propto C(V-V_{th})$$

where Q is one measure of the current flow, C is capacitance, V is the voltage applied to the gate electrode, and V_{th} is the threshold voltage of the device.

To increase the voltage applied to a device requires an increase in power, P ($P \propto V^2$). However, at the same time as increasing the charge in the transistor, subsequent generations also seek to reduce the power required to run the device, since, importantly, a reduction of power reduces the heat generated by the device. Thus, to increase the current flow through the device without increasing the power requires an increase in the capacitance in the gate.

One way to increase the capacitance is by adjusting the thickness of the gate dielectric. In general, the capacitance is related to the gate dielectric by the following formula:

$$C = k_{ox}/t_{electrical}$$

where k_{ox} is the dielectric constant of silicon dioxide (SiO_2) and $t_{electrical}$ is the electrical thickness of the gate dielectric. The electrical thickness of the gate dielectric is greater than the actual thickness of the dielectric in most semiconductor devices. In general, as carriers flow through the channel of a semiconductor-based transistor device there is a quantum effect experienced in the channel which causes an area directly below the gate to become insulative. The insulative region acts like an extension of the gate dielectric by essentially extending the dielectric into a portion of the

channel. The second cause of increase gate dielectric thickness attributable to $t_{\text{electrical}}$ is experienced by a similar phenomenon happening in the gate electrode itself. At inversion, a gate electrode of polysilicon, for example, will generally experience a depletion of carriers in the area of the polysilicon near the gate dielectric. Accordingly, the gate dielectric appears to extend into the polysilicon gate electrode.

The result of the quantum effect in the channel and a depletion in the polysilicon gate electrode is an electrical thickness ($t_{\text{electrical}}$) of the gate dielectric greater than the actual thickness of the gate dielectric. The magnitude of the channel quantum effect and polysilicon depletion may be estimated or determined for a given technology. Accordingly, the electrical thickness ($t_{\text{electrical}}$) for a SiO_2 may be calculated and scaled for a given technology.

In considering the capacitance effects of the gate dielectric, a consideration of the thickness of gate dielectric is important for other reasons. First, the gate dielectric cannot be too thin as a thin gate dielectric will allow a leakage current from the channel through the gate electrode. At the same time, the gate dielectric cannot be too thick because such a gate structure may produce an undesirable fringe electric field. The desired electric field at the gate is typically perpendicular to the surface of the semiconductor substrate. Beyond a certain gate dielectric thickness, generally thought to

be beyond one-third the lateral width of the gate electrode for a SiO₂ gate dielectric, the electrical field deviates from a perpendicular course and sprays about the gate electrode leading to an undesirable fringe electric field.

- 5 What is needed is a way to increase the capacitance of a gate dielectric without decreasing the performance of the device. It is preferable if the increased capacitance is consistent with scaling techniques and may be used in multiple generation technologies.

SUMMARY OF THE INVENTION

A transistor gate dielectric is disclosed. The transistor gate dielectric includes a first dielectric material having a first dielectric constant and a second dielectric material having a second dielectric constant different from the first dielectric constant.

5

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a schematic illustration of a side view of a transistor dielectric having a gate dielectric of a first dielectric material and a second dielectric material.

DETAILED DESCRIPTION OF THE INVENTION

The invention relates to a transistor gate dielectric made up of at least two different dielectric materials. For example, one embodiment contemplates a gate dielectric made up of two different dielectric materials each with its own dielectric constant. The dielectric material nearest the substrate, e.g., a semiconductor substrate will have a modest dielectric constant that produces a defect-free interface with the substrate and is stable against oxide formation. The second dielectric material will have a relatively high dielectric constant and be stable in contact with the desired gate material. By varying the thickness of the material, a gate dielectric can be formed that is scalable for different technology generations, has a low leakage current, and maintains an electric field of the gate perpendicular to the surface of the semiconductor. A transistor gate utilizing the multi-layer gate dielectric is also disclosed.

Figure 1 illustrates an embodiment of the multi-layer gate dielectric of the invention. Figure 1 shows transistor 100 consisting of gate electrode 110 overlying gate dielectric 140. Gate electrode 110 and gate dielectric 140 overlie semiconductor substrate 105 such as, for example, a silicon semiconductor substrate. Formed in substrate 105 adjacent transistor gate electrode 110 are diffusion or junction regions 160. The

transistor is isolated from other devices, in this example, by shallow trench isolation structures 150.

Gate dielectric 140 is made up of, in this example, a bi-layer gate dielectric stack. The gate dielectric material is deposited by conventional techniques such as chemical vapor deposition or other deposition techniques according to the specifics of the material. The individual dielectric materials that make up the gate dielectric stack are patterned using conventional techniques such as masking and etching.

In one embodiment, the bottom dielectric layer 130 is selected to have a modest dielectric constant, k_1 , that forms a generally defect-free interface with substrate 105. A generally defect-free interface is one that has a sufficiently high (e.g., >8 MV/cm) dielectric breakdown strength implying that the dielectric layer is pin-hole free and contains a negligible number of defects that would lead to breakdown of the dielectric layer at lower electric fields. Bottom dielectric layer 130 should also be stable on silicon and stable against oxide formation. In one embodiment, bottom dielectric layer 130 materials are chosen that have a heat of formation greater than the heat of formation of SiO_2 . The chemistry in terms of stability of bottom layer 130 is important to achieve the low defect interface. Examples of suitable bottom dielectric layer 130 include, but are not limited to, hafnium oxide (HfO_2), zirconium oxide (ZrO_2), barium oxide (BaO), lanthanum oxide (La_2O_3), and yttrium oxide (Y_2O_3).

In this embodiment, top dielectric layer 120 is selected to have a relatively high dielectric constant, k_2 , and is a material that is stable in contact with gate electrode 110. Examples of suitable top dielectric layers are BaSrTiO₃ (BST) and PbZrTiO₃ (PZT). One function of top dielectric layer 120 is to block any leakage current through bottom dielectric layer 130, without adding to the equivalent thickness of gate dielectric 140 (i.e., equivalent thickness of an SiO₂ gate dielectric) and contributing to the production of a fringe electric field.

One guideline to select the appropriate dielectric layer thickness t_1 for bottom dielectric layer 130, and t_2 for top dielectric layer 120, is the following. For a given technology generation (i.e., a given gate length of gate electrode 110 and equivalent oxide thickness of a SiO₂ gate dielectric, t_{ox}), a total thickness, t , of gate dielectric 140 should be less than one-third of the gate length of gate electrode 110. The effective dielectric constant, k , may then be determined by the following relationship:

$$k = k_{ox} (t/t_{ox}) \quad (1)$$

wherein k_{ox} is the dielectric constant of SiO₂ which is typically represented as 4.0.

Combining the above relationship with a relationship for calculating the effective dielectric constant of gate dielectric 140 of the following:

$$k = t / (t_1/k_1 + t_2/k_2), \quad (2)$$

the total thickness of dielectric layer 140 may be calculated:

$$t = t_1 + t_2. \quad (3)$$

Combining equations (1), (2), and (3) yields the following:

$$t_1/k_1 + t_2/k_2 = t_{ox}/k_{ox}. \quad (4)$$

Equation (4) is then solved for a thickness of bottom dielectric layer 130 having a known dielectric constant, k_1 , and top dielectric layer 120 also having a known dielectric constant, k_2 . Table I shows the individual thicknesses of first dielectric layer 130 (t_1) and second dielectric layer 120 (t_2) for various technologies scaled by the Morse rule starting with a gate electrode length of 150 nanometers, for a k_1 of 30 and a k_2 of 300.

Table I demonstrates that a multi-layer dielectric gate stack, in this case, a bi-layer dielectric gate stack, is scalable for a given technology. For example, for each technology, given a first dielectric layer 130 having a dielectric constant k_1 of 30 and a second dielectric layer 120 having a dielectric constant k_2 of 300, a total gate dielectric layer thickness less than one-third of the individual gate lengths is maintained. Further, the choice of second gate dielectric layer 120 of material to block the leakage current maintains the performance of the device. Finally, by manipulating the gate dielectric materials, the capacitance of

the device may be appropriately increased for the given technology.

For a gate electrode 110 that is polysilicon, a third dielectric layer may be utilized to act as a barrier layer to prevent interaction between top dielectric layer 120 materials having high dielectric constants and the polysilicon gate material. Suitable third dielectric materials include, but are not limited to, HfO_2 , ZrO_2 , BaO , La_2O_3 , and Y_2O_3 (notably the same materials suitable as bottom dielectric layer 130).

The above example is described with respect to gate electrode 110 being a polysilicon. It is to be appreciated that the same principles may be applied to gate electrodes of different materials, such as, for example, metal gates. In the case of a metal gate electrode, the electrical thickness ($t_{\text{electrical}}$) may be reduced since, in general, metal gate electrodes do not experience the depletion seen by polysilicon. Table I also shows the scaling of the bi-layer dielectric materials discussed above using metal gate technology.

Technology Generation	1	2	3	4	5	6
L_{gate} (nm)	150	100	70	50	35	25
$t_{\text{electrical}}$ (Å)	30	21	15	10	7	5
t_{ox} (Å):metal gate	26	17	11	6	3	1
t (Å):total stack thick	300	210	147	103	72	50
t_1 (Å), $k_1=30$	183	118	75	39	17	3
t_2 (Å), $k_2=300$	117	92	72	64	55	48

Table I

In the preceding detailed description, the invention is described with reference to specific embodiments thereof. It will, however, be evident that various modifications and changes may be made thereto without departing from the broader spirit and scope of the invention as set forth in the claims. The specification and drawings are, accordingly, to be regarded in an illustrative rather than a restrictive sense.

5

CLAIMS

What is claimed:

1. A transistor gate dielectric comprising:
 - a first dielectric material having a first dielectric constant; and
 - a second dielectric material having a second dielectric constant different from the first dielectric constant.
2. The transistor gate dielectric of claim 1, wherein the second dielectric constant is greater than the first dielectric constant.
3. The transistor gate dielectric of claim 1, wherein the first material has a first thickness and the second material has a second thickness, the combination of the first thickness and the second thickness defining a total thickness less than one-third of the length of a transistor gate adapted to overly the gate dielectric.
4. The gate dielectric of claim 3, wherein the first material thickness and the second material thickness are determined by the relationship

$$t_1/k_1 + t_2/k_2 = t_{ox}/k_{ox}$$

wherein t_1 is the first material thickness,
 t_2 is the second material thickness,
 t_{ox} is the minimum thickness for a gate dielectric of
silicon dioxide for a chosen gate length,
 k_1 is the dielectric constant for the first dielectric
material,
 k_2 is the dielectric constant for the second
dielectric material, and
 k_{ox} is the dielectric constant of silicon dioxide.

5. The gate dielectric of claim 1, wherein the first gate
dielectric material is selected from one of silicon nitride,
 HfO_2 , BaO , La_2O_3 , Y_2O_3 , and ZrO_2 .

6. The gate dielectric of claim 1, wherein the second
dielectric material is selected from one of BST and PZT.

7. The gate dielectric of claim 1, further comprising a third
dielectric material having a third dielectric constant.

8. A transistor having a gate electrode overlying a gate
dielectric comprising:

a first dielectric material having a first dielectric
constant; and

a second dielectric material having a second dielectric
constant different from the first dielectric constant.

1 9. The transistor of claim 8, wherein the second dielectric of
2 the gate dielectric has a dielectric constant greater than the
3 first dielectric constant.

1 10. The transistor of claim 8, wherein the first material of
2 the gate dielectric has a first thickness and the second
3 material of the gate dielectric has a second thickness, the
4 combination of the first thickness and the second thickness
5 defining a total thickness less than one-third of a length of
6 the transistor gate electrode.

1 11. The transistor of claim 8, wherein the first material
2 thickness and the second material thickness are determined by
3 the relationship

$$t_1/k_1 + t_2/k_2 = t_{ox}/k_{ox}$$

4 wherein t_1 is the first material thickness,

5 t_2 is the second material thickness,

6 t_{ox} is the minimum thickness for a gate dielectric of
7 silicon dioxide for a chosen gate electrode length,

8 k_1 is the dielectric constant for the first dielectric
9 material,

10 k_2 is the dielectric constant for the second
11 dielectric material, and

12 k_{ox} is the dielectric constant of silicon dioxide.
13

1 12. The transistor of claim 8, wherein the first gate
2 dielectric material is selected from one of silicon nitride,
3 HfO_2 , BaO , La_2O_3 , Y_2O_3 , and ZrO_2 .

1 13. The gate dielectric of claim 8, wherein the second
2 dielectric material is selected from one of BST and PZT.

1 14. The gate dielectric of claim 8, further comprising a third
2 dielectric material having a third dielectric constant.

042390.P5769

ABSTRACT OF THE DISCLOSURE

A transistor gate dielectric including a first dielectric material having a first dielectric constant and a second dielectric material having a second dielectric constant different from the first dielectric constant.

5

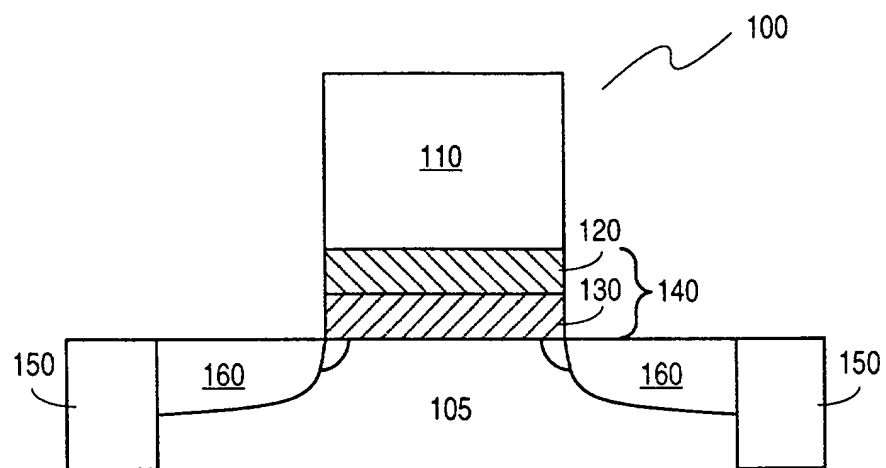
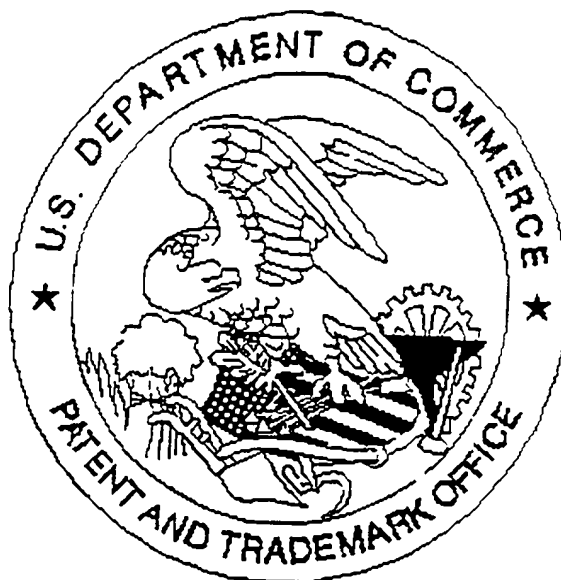


Fig. 1

United States Patent & Trademark Office

Office of Initial Patent Examination -- Scanning Division



Application deficiencies found during scanning:

1. Application papers are not suitable for scanning and are not in compliance with 37 CFR 1.52 because:
 - ☐ All sheets must be the same size and either A4 (21 cm x 29.7 cm) or 8-1/2" x 11". Pages _____ do not meet these requirements.
 - ☐ Papers are not flexible, strong, smooth, non-shiny, durable, and white.
 - ☐ Papers are not typewritten or mechanically printed in permanent ink on one side.
 - ☐ Papers contain improper margins. Each sheet must have a left margin of at least 2.5 cm (1") and top, bottom and right margins of at least 2.0 cm (3/4").
 - ☐ Papers contain hand lettering.
2. Drawings are not in compliance and were not scanned because:
 - ☐ The drawings or copy of drawings are not suitable for electronic reproduction.
 - ☐ All drawings sheets are not the same size. Pages must be either A4 (21 cm x 29.7 cm) or 8-1/2" x 11".
 - ☐ Each sheet must include a top and left margin of at least 2.5 cm (1"), a right margin of at least 1.5 cm (9/16") and a bottom margin of at least 1.0 cm (3/8").
3. Page(s) _____ are not of sufficient clarity, contrast and quality for electronic reproduction.
4. Page(s) _____ are missing.
5. OTHER: No Declaration